REMARKS/ARGUMENTS

Claims 1-17 are pending in the application. Claims 1-17 are rejected. Claims 1, 6, and 9 have been amended.

Claims 1-17 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shen et al. U.S. Patent No. 6,526,481 (Hereinafter "Shen") in view of Barroso et al. U.S. Patent No. 6,668,302 (Hereinafter "Barroso"). Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Barroso in further view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp. 140-240 (Hereinafter "Handy"). Claims 16-17 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Barroso and in further view of Handy and Witt et al. U.S. Patent No. 6,202,139 (Hereinafter "Witt").

Claim Rejections under 35 U.S.C. §112

Claims 1-17 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Specifically, the Office Action states that the integrated cache device was not described in the specification at the time the application was filed. Though Applicants respectfully disagree with this contention, the claims have been amended, removing the objected to phrase.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-17 under 35 U.S.C. §112, first paragraph, are respectfully requested.

Claim Rejections under 35 U.S.C. §103

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shen in view of Barroso. Shen discloses a methodology for designing a distributed shared-memory system. The distributed shared-memory system can incorporate adaptation or selection of cache protocols during operation. It guarantees semantically correct processing of memory instructions by the multiple processors. (*See* Abstract). Barroso discloses a chip-multiprocessing system with scalable architecture included on a single chip.

Applicants respectfully submit that neither Shen, Barroso, nor any combination thereof disclose a cache coherent input/output device. The Office Action cites Barroso as disclosing a single chip device. Shen, which describes a distributed shared memory system, is cited as disclosing the cache coherent device. Shen states:

> Referring still to FIG. 2, memory system 120 includes one cache 130 for each instruction processor 110, and shared-memory system 140. Each cache 130 includes a cache controller 132 and a cache storage 134. Cache storage 134 includes data storage which associates address, data, and status information for a limited portion of the address space accessible from instruction processor 110. Cache controller 132 communicates with memory access unit 117. Memory access unit 117 passes memory access messages to cache controller 132 in response to memory access instructions issued by instruction pool 114. Cache controller 132 processes these memory access messages by accessing its cache storage 134, by communicating in turn with shared-memory system 140, or both. When it has finished processing a memory access message, it sends a result or acknowledgment back to memory access unit 117, which in turn signals to instruction pool 114 that the corresponding memory access instruction has completed.

(Shen, col. 8, line 45–62).

In other words, Shen describes using cache coherency protocols to allow a number of instruction processors to access a distributed cache memory system and not the use of distributed caches for cache-coherent input/output. Therefore claims 1, 6, and 9, are not anticipated by Shen in view of Barroso. Accordingly reconsideration and withdrawal of the rejection of claims 1, 6, and 9 under 35 U.S.C. §103(a) is respectfully requested. In addition, Applicants respectfully

submit that claims 2-4, 7-8, 10-12 and 14 are allowable as depending from allowable base claims 1, 6 and 9.

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Barroso in further view of Handy. Handy discloses a protocol for use in multiple processor system with multiple caches.

As discussed above, Shen and Barroso do not disclose a cache coherent input/output device as recited in claims 1 and 9 as amended, and by their dependency claims 5, 13, and 15. Handy also does not disclose a cache coherent input/output device. Therefore Applicants respectfully submit that claims 5, 13, and 15 are allowable as depending from allowable base claims 1 and 9 given the arguments above.

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Barroso and in further view of Handy and Witt. Witt discloses a pipelined data cache with multiple ports. The invention is described as a computer system including a processor having a cache that includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle. (*See* Abstract, Summary of the Invention, col. 2, ll.31-36)

As discussed above, Shen, Barroso, and Handy do not disclose a cache coherent input/output device as recited in claim 9 as amended, and by their dependency claims 16-17. Witt does not disclose a cache coherent input/output device. Therefore Applicants respectfully submit that claims 16-17 are allowable as depending from allowable base claim 9 given the arguments above.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 16-17 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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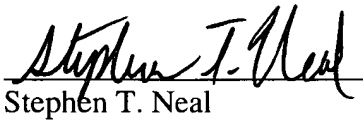
By: 

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